DETAILED ACTION

1.   Claims 31-54 are pending in this application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2.   **Claims 31-48 and 51-53 are rejected under 35 U.S.C. 102(e) as being**

ancitpated by U.S. Pub. No. 2003/0037178 A1 to Vessey et al.

3.   As to claim 31, Vessey teaches a program storage device readable by a

computer, the program storage device tangibly embodying one or more programs of

instructions executable by the computer to perform a method for providing a two-step

communication scheme, the method comprising: establishing a portion of memory

configured to provide asynchronous, connectionless inter-process communication

between a first process and a second processes ("...shared memory...memory

region..." page 2 paragraphs 0024-0028, "...shared memory window..." Main Memory

160 page 5 paragraph 0109, page 6 paragraphs 0121/0130, page 17 paragraphs

0236/0237, page 18 paragraph 0240, page 20 paragraph 0274, figures 22/23 Shared

Memory 160, figure 34 Shared Memory 3460); granting exclusive read and write access

to a first process to the portion of memory configured to provide asynchronous ("…can

write to, and read from…" page 17 paragraphs 0236-0238, "…copies part…" page 17

paragraph 0237, "…read access…write access…" page 18 paragraph 0242, "…access

rights…" page 21 paragraph 0286/0287, "…lock mechanism…acquire lock…" page 21

paragraphs 0289-0292, "…updating information…" page 23 paragraph 0319, "…lock…"

page 22 paragraph 0307), connectionless inter-process communication between the

first process and the second process ("…without…" page 2 paragraph 0024); while

having been granted to the exclusive read and write access to the portion of memory

configured to provide asynchronous, connectionless inter-process communication,

accessing independently of any connection to said second process the portion of

memory configured to provide asynchronous, connectionless inter-process

communication by the first process to modify the contents thereof to provide a message

for processing by the second process ("…without…" page 2 paragraphs 0024-0029,

Shared Memory Driver 2218 page 29 paragraphs 0393/0400, "…emulated socket

connection…" page 32 paragraph 0438, Step 3118 page 26 paragraph 0355); and

releasing exclusive read and write access by the first process to the portion of memory

configured to provide asynchronous, connectionless inter-process communication to

prevent inter-process communication between the first and second process from

becoming a performance bottleneck by releasing resources of the first process after the

first process modifies the contents of the portion of memory ("Deallocate Shared

Memory..." page 26 paragraph 0348, page 27 paragraph 0360).

4.   As to claim 32, Vessey teaches the program storage device of claim 31 wherein

the method further comprises configuring the memory to provide header having an

operation code and a parameter region interpreted according to the operation code

(figure 20 Control Structure header 1910 page 20 paragraph 0278, page 22 paragraph

0302-0304).

5.   As to claim 33, Vessey teaches the program storage device of claim 31, wherein

the providing the message into the portion of memory by the first process further

comprises initiating a remote procedure call ("...procedural parameters..." page 21

paragraph 0278).

6.   As to claim 34, Vessey teaches the program storage device of claim 31 wherein

the method further comprises granting exclusive read and write access to the second

process to the portion of memory configured to provide asynchronous("...access

rights..." page 21 paragraph 0286/0287, "...lock mechanism...acquire lock..." page 19

paragraphs 0289-0292, "...updating information..." page 23 paragraph 0319, "...lock..."

page 22 paragraph 0307), connectionless inter-process communication , while having

been granted to the exclusive read and write access to the portion of memory,

accessing independently of any connection to said first process the portion of memory

by the second process ("…without…" page 2 paragraphs 0024-0029, Shared Memory

Driver 2218 page 29 paragraphs 0393/0400, "…emulated socket connection…" page 32

paragraph 0438) to access the message provided in the portion of memory by the first

process (Steps 3136-3146 page 27 paragraph 0359) and releasing exclusive read and

write access by the second process to the portion of memory page ("Deallocate Shared

Memory…" page 26 paragraph 0349, page 27 paragraph 0360).

7.   As to claim 35, Vessey teaches the program storage device of claim 34 wherein

the method further comprises: establishing exclusive read and write access to the

portion of memory by the second process ("…access rights…" page 21 paragraph

0286/0287, "…lock mechanism…acquire lock…" page 19 paragraphs 0289-0292,

"…lock…" page 22 paragraph 0307); accessing independently of any connection to said

first process the portion of memory by the second process to provide a result message

in response to the message placed in the portion of memory by the first process

("…without…" page 2 paragraphs 0024-0029, Shared Memory Driver 2218 page 29

paragraphs 0393/0400, "…emulated socket connection…" page 32 paragraph 0438);

releasing exclusive read and write access by the second process to the portion of

memory ("Deallocate Shared Memory…" page 26 paragraph 0349, page 27 paragraph

0360) and providing by the second process a notification to the first process to check

the portion of memory ("…inter-processor interrupt mechanism…" page 20 paragraph

0274, "…to alert…" page 23 paragraph 0322, page 24 paragraphs 0328/0329, "Send

Signal…" page 26 paragraph 0349).

8.   As to claim 36, Vessey teaches the program storage device of claim 31 wherein

the method further comprises providing by the first process a notification to the second

process to check the portion of memory ("OS1 copies the offset pointer..." page 19

paragraph 0256, "...inter-processor interrupt mechanism..." page 20 paragraph 0274,

"...to alert..." page 23 paragraph 0322, page 24 paragraphs 0328/0329, "Send

Signal..." page 26 paragraphs 0349/0355).

9.   As to claim 37, Vessey teaches a server comprising a memory (figures 22-24),

wherein a portion of the memory is configured to provide two-step, asynchronous,

connectionless inter-process communication between a first process and a second

process, the portion of memory being configured as memory accessible by the first and

second processes by selective granting ("...shared memory...memory region..." page 2

paragraphs 0024-0028, "...shared memory window..." Main Memory 160 page 5

paragraph 0109, page 6 paragraphs 0121/0130, page 17 paragraphs 0236/0237, page

18 paragraph 0240, page 20 paragraph 0274, figures 22/23 Shared Memory 160, figure

34 Shared Memory 3460), wherein read and write access to the portion of memory

being granted exclusively to the first process for modification of contents of the portion

of memory independently of any connection to said second process ("...without..." page

2 paragraphs 0024-0029, Shared Memory Driver 2218 page 29 paragraphs 0393/0400,

"...emulated socket connection..." page 32 paragraph 0438) to prevent inter-process

communication between the first and second process ("... "exclusive window"..." page 6

paragraphs 0123/0128/0129, "…access rights…" page 21 paragraph 0286/0287,

"…lock mechanism…acquire lock…" page 21 paragraphs 0289-0292, "…lock…" page

22 paragraph 0307) from becoming a performance bottleneck by releasing resources of

the first process after the first process modifies the contents of the portion of memory

("Deallocate Shared Memory…" page 26 paragraph 0349, page 27 paragraph 0360).

10.   As to claims 38 and 44, see the rejection of claim 32 above.

11.   As to claims 39 and 45, see the rejection of claim 33 above.

12.   As to claim 40, Vessey teaches the server of claim 37, wherein the first process

releases exclusive read and write access by the first process to the portion of memory

("Deallocate Shared Memory…" page 26 paragraph 0349, page 27 paragraph 0360),

the second process is granted exclusive read and write access to the portion of memory

configured to provide asynchronous ("…access rights…" page 21 paragraph 0286/0287,

"…lock mechanism…" page 19 paragraph 0289, "…updating information…" page 23

paragraph 0319, "…lock…" page 22 paragraph 0307), connectionless inter-process

communication, accesses the portion of memory independently of any connection of

said first process to access the message provided in the portion of memory by the first

process ("…without…" page 2 paragraphs 0024-0029, Shared Memory Driver 2218

page 29 paragraphs 0393/0400, "…emulated socket connection…" page 32 paragraph

0438) and releases exclusive read and write access by the second process to the

portion of memory ("Deallocate Shared Memory..." page 26 paragraph 0349, page 27

paragraph 0360).

13.   As to claim 41, see the rejection of claims 35 and 36 above.

14.   As to claims 42 and 48, see the rejection of claim 36 above.

15.   As to claim 43, Vessey teaches a system (figures 22-24), comprising: a first

process (OS1 2206a/APP1 2208a); a second process (OS1 2206n/APP1 2208n); and

memory configured to provide asynchronous, inter-process communication between the

first process and the second process, wherein read and write the memory provides a

portion of memory configured to be accessible by the first and second processes

("...shared memory...memory region..." page 2 paragraphs 0024-0028, "...shared

memory window..." Main Memory 160 page 5 paragraph 0109, page 6 paragraphs

0121/0130, page 17 paragraphs 0236/0237, page 18 paragraph 0240, page 20

paragraph 0274, figures 22/23 Shared Memory 160, figure 34 Shared Memory 3460) by

selective granting ("...access rights..." page 21 paragraph 0286/0287, "...lock

mechanism..." page 19 paragraph 0289, "...updating information..." page 23 paragraph

0319, "...lock..." page 22 paragraph 0307), wherein read and write access to the portion

of memory is granted exclusively to the first process for modification of contents of the

portion of memory to prevent inter-process communication between the first and second

process ("...lock mechanism...acquire lock..." page 21 paragraphs 0289-0292,

"…updating information…" page 23 paragraph 0319, "…lock…" page 22 paragraph

0307) from becoming a performance bottleneck by releasing resources of the first

process after the first process modifies the contents of the portion of memory

("Deallocate Shared Memory…" page 26 paragraph 0349, page 27 paragraph 0360).

16.   As to claim 46, see rejection of claim 34 above.

17.   As to claim 47, Vessey teaches the system of claim 46, wherein the second

process is granted exclusive read and write access to the portion of memory, accesses

the portion of memory to provide a result message in response to the message placed

in the portion of memory by the first process ("…access rights…" page 21 paragraph

0286/0287, "…lock mechanism…acquire lock…" page 21 paragraphs 0289-0292,

"…updating information…" page 23 paragraph 0319, "…lock…" page 22 paragraph

0307), releasing exclusive read and write access by the second process to the portion

of memory ("Deallocate Shared Memory…" page 26 paragraph 0349, page 27

paragraph 0360) and provides a notification to the first process to check the portion of

memory ("…inter-processor interrupt mechanism…" page 20 paragraph 0274, "…to

alert…" page 23 paragraph 0322, page 24 paragraphs 0328/0329, "Send Signal…"

page 26 paragraph 0349).

18.   As to claims 51-53, see the rejection of claim 1 above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

19.   Claims 49, 50 and 54 are rejected under 35 U.S.C. 103(a) as being

unpatentable over U.S. Pat. No. 6,804,714 B1 to Tummalapalli in view of U.S. Pat.

No. 2003/0037178 A1 to Vessey et al.

20.   As to claim 49, Tummalapalli teaches a service level agreement (SLA) server,

comprising: a plurality of processes (figure 2 Col. 5 Ln. 25 – 67), the plurality of

processes comprising a database manager for managing performance data, an

application server for collecting performance data ("…concurrent processing server…"

Col. 5 Ln. 45 – 65, Col. 7 Ln. 1 – 6) and providing a client interface for establishing

service level agreements (User Layer tool 236/Service Reports tool 234 Col. 8 Ln. 45 –

53), a SLA core for analyzing data and controlling actions based on service level

agreements and policy ("…concurrent processing managers…" Col. 5 Ln. 45 – 67, Col.

6 Ln. 66 – 67, Col. 7 Ln. 1 – 20) and a performance monitor daemon for communicating

with remote I/O service gateways to collect data and send throttling requests

("Database performance monitor…" Col. 6 Ln. 42 – 59);

Tummalapalli is silent with reference to memory configured to provide asynchronous, inter-process communication between the processes, wherein the memory provides a portion of memory configured to be accessible by the processes by selective granting, wherein read and write access to the portion of memory is granted exclusively to a first of the processes for modification of contents of the portion of memory to prevent inter-process communication between the process from becoming a performance bottleneck by releasing resources of the first of the processes after the first of the processes modifies the contents of the portion of memory.

Vessey teaches a memory configured to provide asynchronous, inter-process communication between the processes, wherein the memory provides a portion of memory configured to be accessible by the processes by selective granting ("...shared memory...memory region..." page 2 paragraphs 0024-0028, "...shared memory window..." Main Memory 160 page 5 paragraph 0109, page 6 paragraphs 0121/0130, page 17 paragraphs 0236/0237, page 18 paragraph 0240, page 20 paragraph 0274, figures 22/23 Shared Memory 160, figure 34 Shared Memory 3460), wherein read and write access to the portion of memory is granted exclusively to a first of the processes for modification of contents of the portion of memory to prevent inter-process communication between the process ("...access right..." page 7 paragraph 0131, "...copies part..." page 17 paragraph 0237, "...access rights..." page 21 paragraph 0286/0287, "...lock mechanism...acquire lock..." page 21 paragraphs 0289-0292, ...updating information..." page 23 paragraph 0319, "...lock..." page 22 paragraph 0307) from becoming a performance bottleneck by releasing resources of the first of the

processes after the first of the processes modifies the contents of the portion of memory

("Deallocate Shared Memory…" page 26 paragraph 0349, page 27 paragraph 0360).

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the teachings of Vessey and Tummalapalli because the

teaching of Vessey would improve the system of Tummalapalli by providing a locking

mechanism for locking shared memory in order to facilitate greater throughput between

partitions, since contention for system lock is eliminated (Vessey page 22 paragraph

0307).

21.   As to claims 50 and 54, see the rejection of claim 49 above.

Response to Arguments

Applicant's arguments filed 7/4/08 have been fully considered but they are not

persuasive.

Applicant argues in substance that (1) the Vessey prior art does not teach

connectionless inter-process communication between a first and second processes and

(2) the Vessey does not also teach a portion of memory configured to be accessible by

a first and second processes by selective granting access, whereby the read and write

access to the portion of memory is granted exclusively to the first process.

Examiner respectfully traverses Applicant's arguments:

As to point (1), the Vessey prior art discloses a method of emulating network

communications between applications executing in different partitions of a partitionable

computer system. A connection is established between a first partition and a second partition of a computer system, through a memory region of the computer system shared by both the first partition and the second partition. Network messages are transmitted from a first application in the first partition using a network application interface and intended for transmission to a second application in the second partition. The network messages transmitted by the first application are transmitted to the second application via the connection established through the memory region. This technique allows applications in different partitions of the computer system to communicate using the networking application interfaces, **but without the need for an external network connection between the partitions**. The shared memory resources of a partitionable computer system enables the emulate network communications through a region of memory shared by one or more partitions. The emulate network communications and therefore "connection between partitions without the need for an external network connection" makes the communication between partitions connectionless.

As to point (2), as discussed above the Vessey prior art discloses a method of emulating network communications between applications executing in different partitions of a partitionable computer system using shared memory region. Access to the shared memory region is controlled by a lock mechanism. The lock mechanism allows the different partitions to lock access to the memory structures of shared memory region as needed and ensures that one partition is capable modifying any memory structure at any given time and therefore allows for exclusive/selective granting of access to the shared memory region.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Charles E. Anya whose telephone number is 571-272-

3757. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

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